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OPTIMAL CONFIGURATION OF DIGITAL DOWN CONVERTER IN COMMUNICATION SYSTEM

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Abstract

In this paper we discuss the efficient modeling flow from Xilinx 10.1 ISE Simulator to FPGA. FPGAs allow to experiment and evaluate the best implementation architecture. Due to their re-programmability, the rigorous verification and testing procedures required at various stages of hardware development can be relaxed. We show the reference design of Digital Down Converter in a core technology by integrating Matlab with ISE design tool. Here the RF signal is converted to the IF signal, and then decimated at a programmable rate using CIC filter, where the same data can be obtained at output as that of source with the down sampling conversion techniques. The main advantage of using an Xilinx 10.1 ISE Simulator to work and to support all types of IP cores flexibly. The data is commonly taken directly from analog to digital converters (ADC's) sampling at tens or hundreds of MHz, which is beyond the real time computational capabilities of software processors. A DDC consists of a cascaded integrated comb filters, a mixer, and a direct digital synthesizer (DDS). These filters are designed using Matlab and developed VHDL code. Simulation and functional verification is carried out using Xilinx ISE and, FPGA implementation on Virtex-II Pro. The CIC decimation Filter is a programmable filter increases the sampling rate. Mixer is designed with an area efficient high-speed algorithm for variable multiplication and generation of carrier waves with a wide range of frequencies from the Direct Digital Synthesizer.

Keywords : Digital Down Converter, Digital Direct Synthesizer, Mixer, CIC filter